Low Noise Preamplifier for THz Detector

Anyi Rao

(2014', School of Electronic Science and Engineering, Nanjing University, Nanjing 210023)

Mentor: Lin Kang

(School of Electronic Science and Engineering, Nanjing University, professor,Nanjing 210093)

Abstract: Terahertz technology has important promising applications in the imaging radar, medical diagnosis, battlefield target identification, etc. However, due to the lack of high sensitive and accurate detector, terahertz technology's application is limited. A low noise amplifier is essential part to this problem. The goal of this paper is to design a low noise and accurate preamplifer. My goal is achieved by employing a differential input structure, which greatly improves the noise performance. The requirement of this design is controlling the preamplifer's noise performance less than 10nV/$\sqrt{Hz}$ to satisfy THz detector Data acquisition circuit's resolution. Preamplifer's input signal has a 4kHz center frequency with 1kHz bandwidth, 100μV-1mV amplitude. Its output signal amplitude needs to greater than 100mV.

Keywords: preamplifier; noise

1 Introduction

THz detector application's block diagram is shown in Figure 1. Preamplifier's design and optimization are needed. Considering the main source of noise is 50Hz power interference noise, active device noise and inactive devices[1] ($\frac{1}{f}$ noise, broadband white noise, etc.), there are two designs:

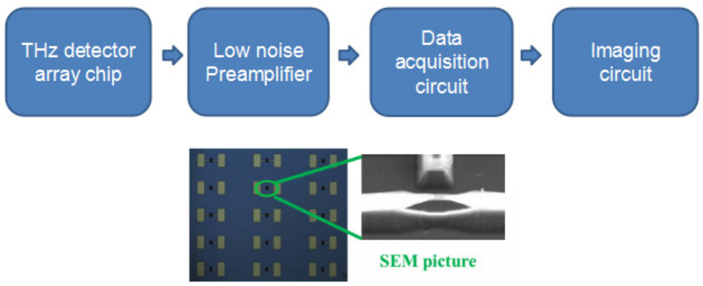


Figure 1: Block diagram of THz detector

1.1 Design 1 Two Stage Band-pass Filter

Input stage is a Delyiannis Band-pass Filter[3], as shown in Figure 2.

Then write down the node voltage formulas of this circuit.

$$\begin{cases} (\frac{1}{R_1}+\frac{1}{R_3}+SC_1+SC_2)V_1-\frac{1}{R_1}V_i-SC_1V_2-SC_2V_0=0 \\ (\frac{1}{R_2}+SC_2)-\frac{1}{R_2}V_o-SC_1V_1=0 \\ V_2=0 \end{cases}$$

Transfer function H(s)= $\frac{V_O}{V_i}=\frac{-S/R_1C_2}{S^2+S(\frac{1}{R_2}(\frac{1}{C_1}+\frac{1}{C_2}))+\frac{1}{R_2C_1C_2}(\frac{1}{R_1}+\frac{1}{R_3})}$

Stage II uses wide band band-pass filter, as shown in Figure 3.

Transfer function H(s)= $\frac{V_O}{V_i}=-\frac{R_4\|\frac{1}{SC_1}}{\frac{1}{SC_2}+R_3}$

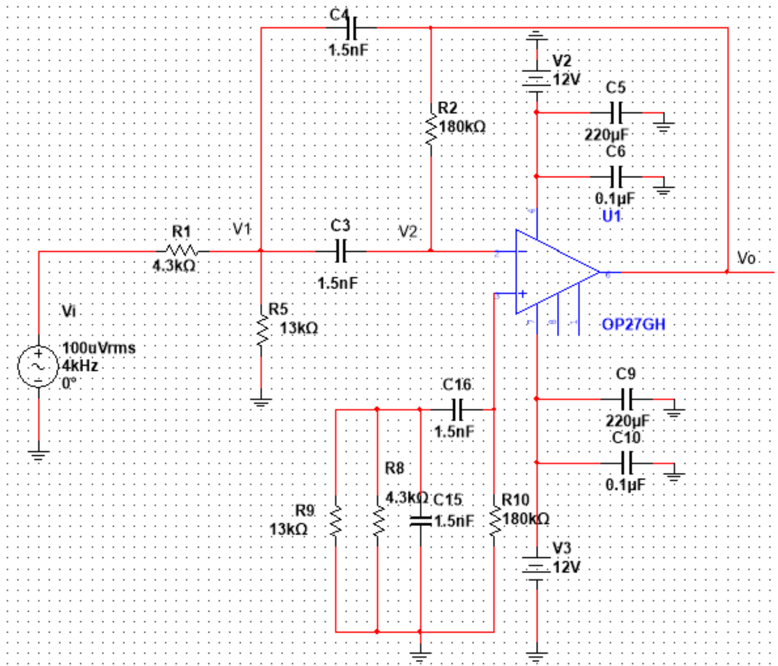


Figure 2: Input stage Delyiannis Band-pass Filter

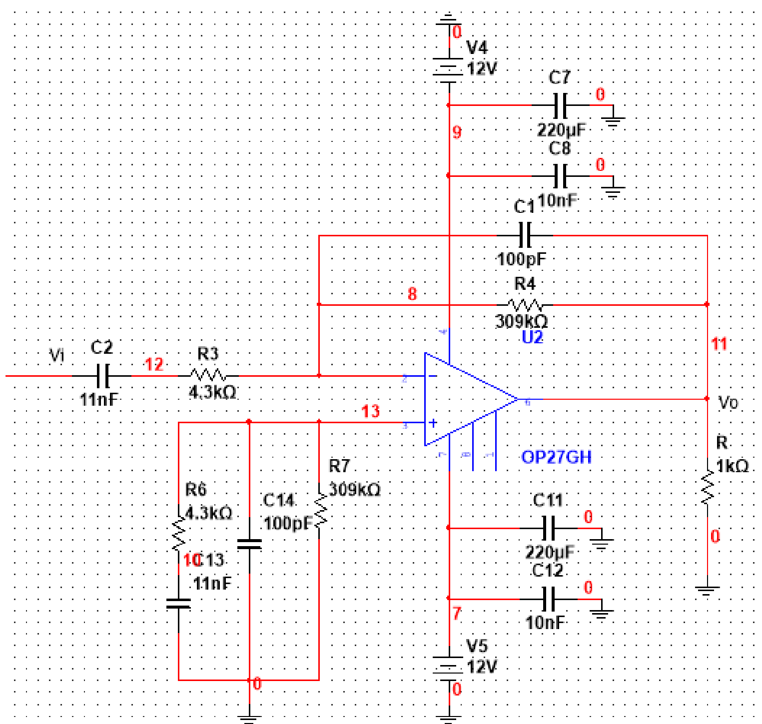


Figure 3: Wide band band-pass filter

1.2 Design 2 The Combination of Instrumental Amplifier and Band-pass Filter

Input stage is a differential input circuit, in which Op Amp 1 and Op Amp 2 configurate the first level. Op Amp is the second level, as shown in Figure 4.

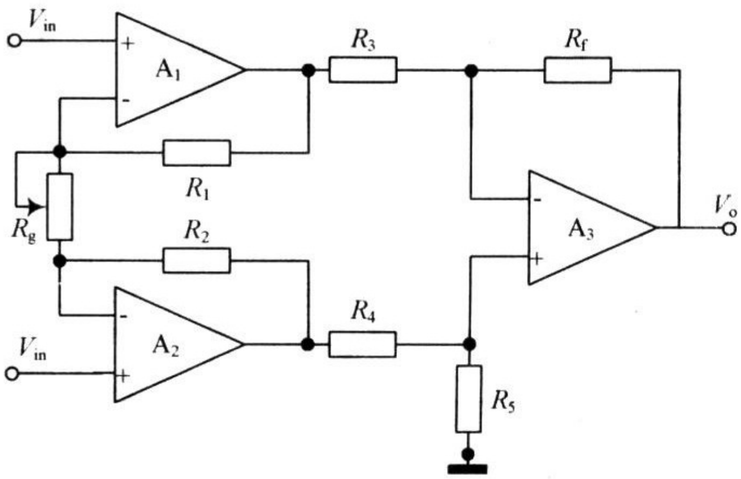


Figure 4: Differential input circuit

Transfer function H=$\frac{V_O}{V_{in1}-V_{in2}} = -\frac{R_5}{R_3}(1+2\frac{R_1}{R_g})$ Stage II is the Delyiannis band-pass filter of feedback structure. The schematic diagram is shown in Figure 5.

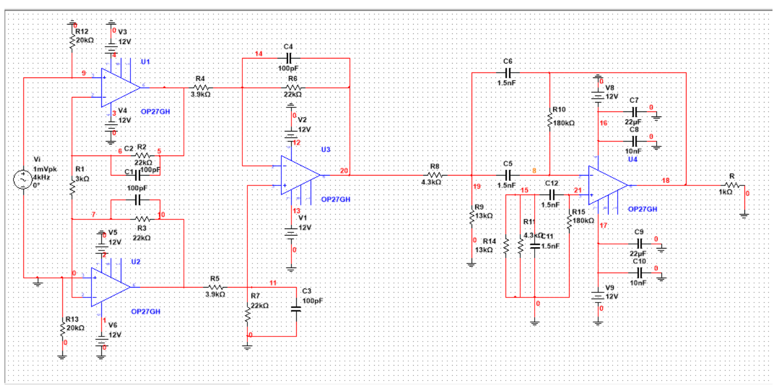


Figure 5: Design 2

1.3 Notices in the Process of Experiment

Selection of Op Amp chips: Considering the noise of chips and the cost of the experiment, I use OP27G comparing with other chips because of coefficient factor.[1]

Selection of resistors: Metal film resistor.

It is of small size, low noise, good stability, but the cost is higher, allowing the error is

[1]Because the experiment is studies the pros and cons of different method, the experiment is meaningful as long as the Op Amp chip doesn't loss the generality.

Item	Frequency	typ max
Input voltage noisee_nnV/ $\sqrt{Hz}$	f=10Hz	3.8 8.0
	f=30Hz	3.3 5.6
	f=1000Hz	3.2 4.5
Input current noisee_nnA/ $\sqrt{Hz}$	f=10Hz	1.7 –
	f=30Hz	1.0 –
	f=1000Hz	0.4 0.6
Gain of band width (GBW)	f	5.0 8.0

Table 1: Chip Parameters

±0.5%.

Selection of capacitors: Ceramic capacitor and electrolytic capacitor.
Ceramic capacitor has a lower capacitance value generally , while the electrolytic capacitor's capacitance value is generally larger.

The symmetrical design: Due to the introduction of the negative feedback, Op Amp inverting terminal grounds directly. Therefore, it will lead the noise from land into the amplifying circuit. Obviously, this isn't what we expect. Accordingly it connects the resistors and capacitors which are the same as the in-phase terminal causing a symmetrical structure. The structure can inhibit the inverting and non-inverting input common mode signal, then restrain the noise.

Op Amp power supply decoupling design: Because Op Amp's power supply comes directly from the power box, so the fluctuations of the amplitude of power voltage will affect Op Amp performance to a certain extent. Accordingly, it uses two small capacitors in parallel way to remove the interference of the high-frequency and low-frequency noise.[2]

[2]In addition, there are many points needed to pay attention, such as PCB layout drawing, the practical operation process, which will be described in later.

f_0/kHz	BW/kHz	A_0
4.0	1	1500

Table 2: Theoretical Calculation of Design 1

f_0/kHz	BW/kHz	A_0
4.0	1.02	1500.4

Table 3: Multisim Simulation Experiment of Design 1

2 Theoretical Calculation and Multisim Simulation

2.1 Design 1

The resistance capacitance values is shown in Figure 6. According to the theoretical formula, we get Table 2.

From Multisim Simulation,AC Analysis, I get Table 3.

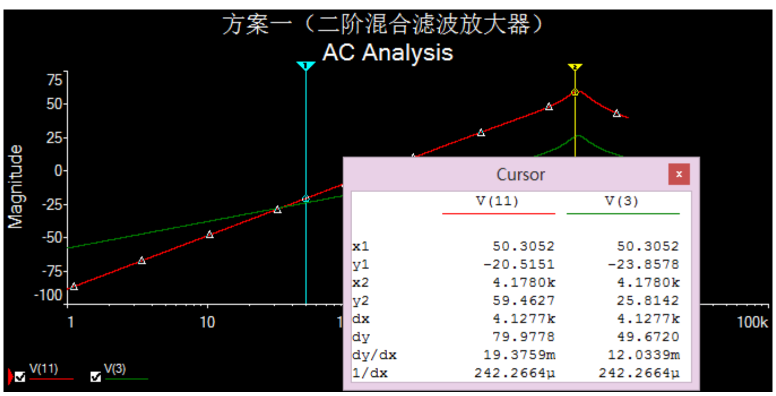


Figure 6: Instrumentation Amplifier

From Figure 6, V_3 shows the amplitude frequency response of input stage (Delyiannis Filter, V_{11} shows the total amplitude frequency response.

The restrain to 50Hz signal in the input reaches -79.9778dB, namely it reduces noise by 1×10^4. This is exactly what we need.

f_0/kHz	BW/kHz	A_0
4.0	1	2000

Table 4: Theoretical Calculation of Design 2

f_0/kHz	BW/kHz	A_0
4.0	0.99	1997.5

Table 5: Multisim Simulation Experiment of Design 2

2.2 Design 2

The value is shown in Figure 5, and Table 4 is got according to theoretical formula. Table 5 is got according to Multisim AC Analysis, Figure 7 V_{18} shows the amplitude

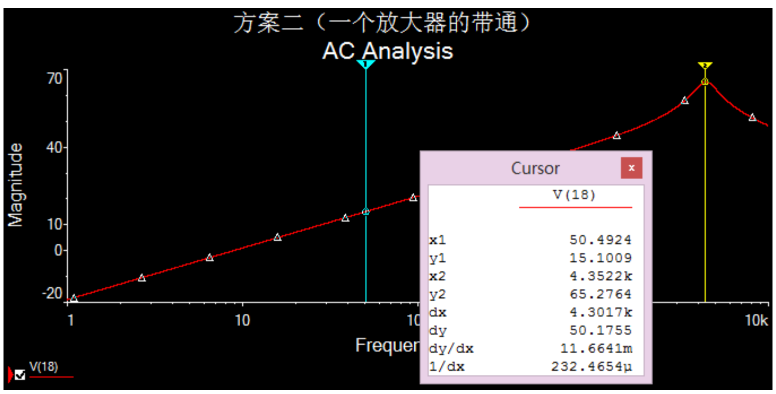


Figure 7: Differential input amplifier

frequecy response of output in logarithmic representation

The restrain to 50Hz signal in the the output is -50.1755dB, which is worse than design 1. But Design 2 uses differential input, which has high common mode rejection ratio. This properity makes things better.As shown in Figure 8, I measure the common mode gain when I put the 1V 50Hz noise signal in both input terminal.

And we get V_o=V_{18}=204.1nV

$\because$ V_2=V_5=1V

$\therefore$ A_c=$\frac{V_o}{V_i}$=2.041×10^{-7}

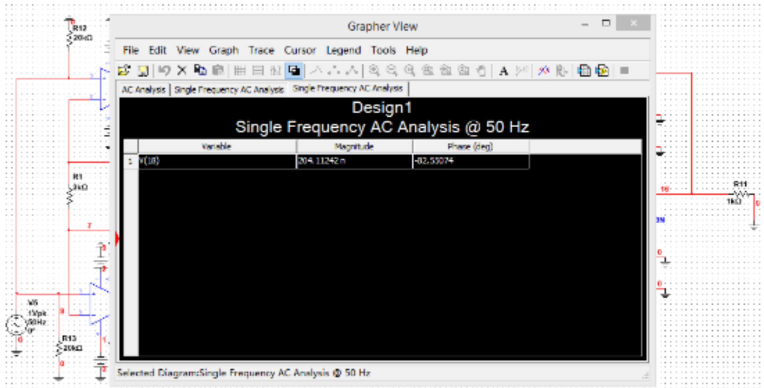


Figure 8: Common-mode Voltage Gain

2.3 Theoretical Noise Analysis of Amplifier

From the device manual of OP27-G[4], as shown in Figure 9, OP27-G $\frac{1}{f}$ normalized voltage noisee_{form}=1.2nV/ $\sqrt{Hz}$, wide width white voltage noisee_{BB}=3nV/ $\sqrt{Hz}$, wide width white current noisee_{inBB}=0.3pA/ $\sqrt{Hz}$

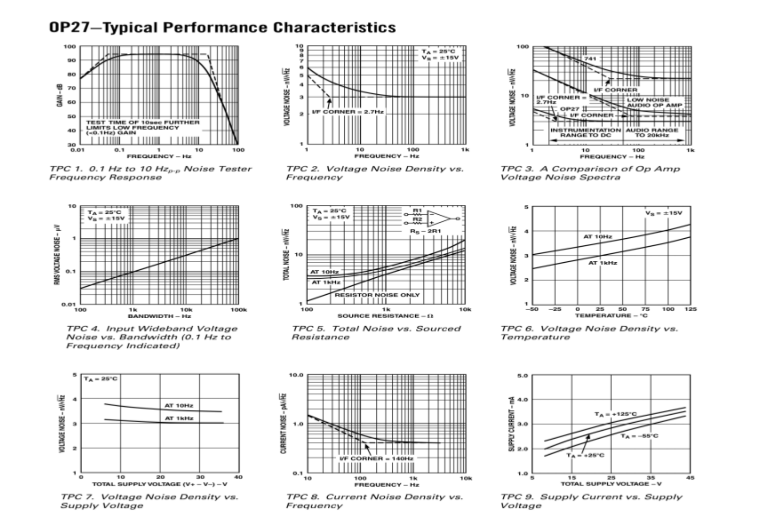


Figure 9: OP27-G Noise performance from device manual

2.3.1 Design 1

Configurate the Thevenin equivalent circuit by using Multisim. The input resistence is R_{eq}=$\frac{U_x}{I_x}$=$\frac{U_i - I_x R_s}{I_x}$=1.468kΩ

Voltage noise $\frac{1}{f}$noise: e_f=$e_{form}\sqrt{ln\frac{f_H}{f_L}}$=3.7nV

wide width white voltage noise

e_{nBB}=$e_{BB}\cdot\sqrt{BW_n}$=118.8nV

e_{n-v}=$\sqrt{e_f^2+e_{nBB}^2}$=118.9nV

Current noise Consider the wide width white current noise

e_{n-i}=$R_{eq}\cdot e_{inBB}\cdot\sqrt{BWn}$=17.5nV, and the $\frac{1}{f}$noise of current is small enough to be ignored.

Resistors thermal noise e_{n-R}=$\sqrt{4KTR_{eq}BW_n}$=0.197μV

（where k is Boltzman constant, t is temperature in Kelvin's scale）

e_{n-RTL}=$\sqrt{e_{n-v}^2+e_{n-i}^2+e_{n-R}^2}$=0.230$\mu$V

2.3.2 Design 2

The noise model of differential circuit is shown in Figure 10.

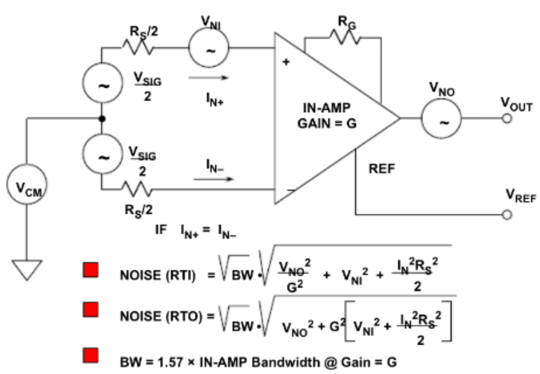
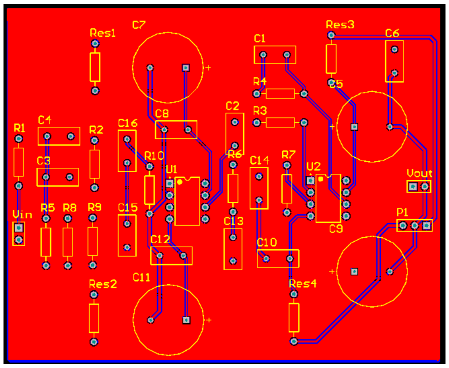


Figure 10: Differential Circuit Noise

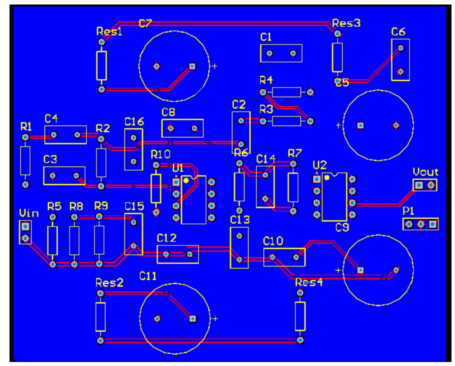
NOISE(RTL)=914.39nV

Delyiannis band pass filter is both used in design 1 and design 2.

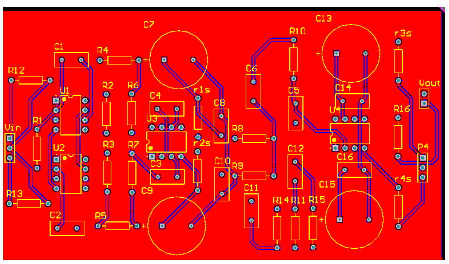
e_{n-RTL}=$\frac{N1G1G2+N2G2}{G1G2}$=N1+$\frac{N2}{G1}$=0.915μV



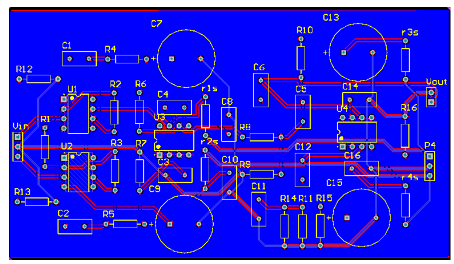
(a) 1 top layer



(b) 1 bottom layer



(c) 2 top layer



(d) 2 bottom layer

Figure 11: The PCB

2.4 Deficiencies of Theoretical Noise Analysis

Theoretical analysis only considers the noise of Op Amp. There are lots of factors which are not included in, such as that the power line will conduct noise, ground plane will conduct noise, and the air radiation noise. Hence, the low Op Amp noise is advantageous to subsequent practical PCB circuit product and practical experiment. And this paper will continue to discuss the noise in the following practical experiment.

3 Practical Experiment

Apparatus Oscilloscope Tektronix TDS1012B-SC, power GWINSTEKGPO-33030, signal source KEITHLEY3390, multimeter FLUKE8808A.

Temperature T=25°C

PCB Picture The width of power line and ground line is 20mil, as shown in Figure 11. Especially the symmetry of design 2 is better than design 1, the wires between different layers is orthogonal.

After getting the actual PCB, weld the component and PCB according to the schematic diagram. Then measure the experimental data of design 1, as shown in Table 6.

f/kHz	1.0	1.5	2.0	2.5	3.0	3.1	3.2	3.3	3.4	3.5
V_{p-p}/V	0.07	0.15	0.26	0.44	0.74	0.84	0.84	1.06	1.18	1.30
f/kHz	3.6	3.7	3.8	3.9	4.0	4.1	4.2	4.3	4.4	4.5
V_{p-p}/V	1.45	1.66	1.74	1.80	1.80	1.76	1.68	1.58	1.46	1.34
f/kHz	4.6	4.7	4.8	4.9	5.0	5.5	6.0	6.5	7.0	8.0
V_{p-p}/V	1.26	1.18	1.08	1.04	1.02	0.78	0.61	0.50	0.44	0.37

Table 6: Design 1 Magnitude ResponseV_{ip-p}=1.08 mV

Poly the data by MATLAB, as shown is Figure 12.

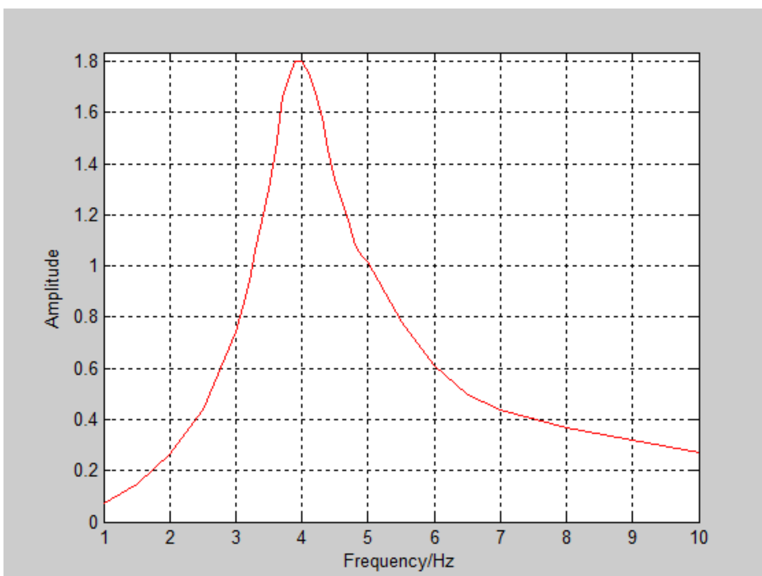


Figure 12: Magnitude Response of Design 1

Taylor expand the amplitude frequency response between 3kHz-5kHz

f(x)=$-0.2342\times x^5+5.7029\times x^4+-53.3265\times x^3+240.4312\times x^2-524.0543\times x+443.8479$

f'(x)=$-(1171\times x^4)/1000+(57029\times x^3)/2500-(22515113018341197\times x^2)/140737488355328+$

$(264356900080137\times x)/549755813888-2304815185744049/4398046511104$

Solve f'(x)=0

x=3.9712

It is coherent with the theory.

Then measure the circuit and get the experimental data of design 2, as shown in Table 7.

f/kHz	1.0	1.5	2.0	2.5	3.0	3.1	3.2	3.3	3.4	3.5
V_{p-p}/V	0.21	0.38	0.48	0.71	1.10	1.22	1.31	1.44	1.58	2.08
f/kHz	3.6	3.7	3.8	3.9	4.0	4.1	4.2	4.3	4.4	4.5
V_{p-p}/V	2.32	2.56	2.76	2.88	2.96	2.92	2.84	2.682	.58	2.36
f/kHz	4.6	4.7	4.8	4.9	5.0	5.5	6.0	6.5	7.0	8.0
V_{p-p}/V	2.16	2.04	1.98	1.86	1.64	1.18	1.16	1.02	0.84	0.70

Table 7: Design 2 Magnitude ResponseV_{ip-p}=1.45mV

Poly the data by MATLAB, as shown is Figure 13.

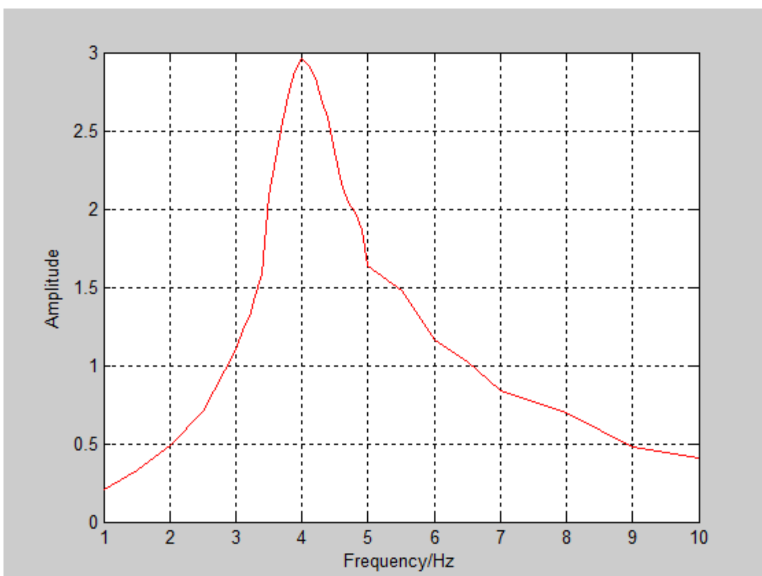


Figure 13: Magnitude Response of Design 2

Taylor expand the amplitude frequency response between 3kHz-5kHz.

f(x)=$1.7369 \times x^4 - 27.8764 \times x^3 + 164.5621 \times x^2 - 422.6665 \times x^1 + 400.0305$

f'(x)=$(17369\times x^3)/2500-(209073\times x^2)/2500+(1447503539529895\times x)/4398046511104-7435627702742155/17592186044416$

f_0/kHz	V_{imax}	V_{omax}	A_c	K_{CMR}/dB	
50	1	0.718	7.18×10^4	2.04×10^3	129

Table 8: Common-mode Voltage Gain and Common-mode Rejection Ratio

Design	$V_{o-noise}/mV$	BW/kHz	A_o	A_e	$V_{i-noise}/\mu V$
1	1.302	1.3	1.67×10^3	20.8	62.6
2	0.212	1.3	2.04×10^3	27.6	7.68

Table 9: Noise Analysis

Solve f'(x)=0

x=4.0632

It is coherent with the theory.

4 Noise Analysis

Complete the circuit and ensure it working normally. Then the input terminal is grounded, and the output voltage is measured by the multimeter FLUKE8808A, recording the maximum value of the output voltage.

Take advantage of $BW_{equip} \times A_e = BW \times A_o \times k$ and calculate the equivalent magnification A_e, where BW_{equip} is measurable bandwidth of FLUKE8808A BW_{equip} =150kHz， BW is the bandwidth of the circuit, k is an empirical value, A_o is the center frequency of the amplification circuit[2].

Carrying out measurement to design 1 $V_{o-noise} = 1.302mV$

Carrying out measurement to design 2 $V_{o-noise} = 0.212mV$

It can be seen from the comparison as shown in Table 9, the equivalent noise of design 2 is better than design 1, because the design 2 uses the differential input mode, sacrificing two times the components than design 1 for the better effects.

Though the design 1, which sets filtering as its main target, is better in theoretical analysis and simulation, it is difficult to get rid of the practical noise from each circuit stage in practical experiment process. And it is easy to control the noise in the practical

Design	theory	Multisim	experiment	error
1 Amplitude Maximum value A_o	1.5×10^3	1.5004×10^3	1.67×10^3	11.3%
2 Amplitude Maximum value A_o	2.0×10^3	1.9975×10^3	2.04×10^3	2.0%
$2K_{CMR}$/dB	–	199.69	129	35.4%

Table 10: Error Analysis

experiment because of its symmetry. Therefore, design 2 has more advantages. [3]

Additionally, When drawing PCB, design 2 is easy to be mirror-symmetrical because of the differential input mode. This enhances the effect of symmetrical design.

5 Error Analysis

In order to make the experiment more convincing, it introduces a small signal in the input terminal by using series connecting allotting circuit. This circuit will cause additional error to the experiment. Measurement is carried out, as shown in Table 10. The error of design 2 is smaller than design 1.

6 Conclusions

Deficiencies The empirical formula for noise analysis $BW_{equip} \times A_e = BW \times A_o \times k$ is not the best, though it is efficient. Because in the noise analysis, the most important thing is to get the equivalent input noise. Assuming the relationship between the voltage of input noise signal and the frequency can be depicted by function f (x), the relationship between the magnification and the frequency can be depicted by function g(x). After amplifier circuit's effect, the relationship between the voltage of output noise signal and the frequency can be depicted by the function H (x). Therefore, the measured voltage of output noise by multimeter FLUKE8808A is $V_{o-noise} = \int h(x)dx = \int f(x) \cdot g(x)dx$

$V_{o-noise}$ and g（x）is given, by calculating $V_{i-noise} = \int f(x)dx$, the accurate value will be

[3] Taking an overview of the two design, in order to get larger amplification and make the result more obvious, the experiment uses higher resistance values. This will introduce a greater resistance thermal noise, which is disadvantageous to the overall noise.

got.

Expectation In agreement with other functions, the noise performance can be improved to two order of magnitude (100 times). Therefore, the differential input mode will have a broad prospect, and it will be applied to the THz detector and it can used in practical way to a certain extent, so the THz technology will have further application.

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